Parallelisation of Digital Signal Processing in Uniform and Reconfigurable Filter Banks for Satellite Communications

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Abstract—Modern satellite communication calls for novel and flexible concepts for de- and remultiplexing of wide-band FDM-signals in conjunction with beam switching on-board a satellite. For this application, two highly efficient approaches to uniform and yet reconfigurable digital filter banks are known:

i) the complex-modulated polyphase filter bank, and

ii) the tree-structured filter bank.

Channelising and remultiplexing of (ultra-)wide-band FDM-signals require high end sample rates that, often, range beyond technological limit (e.g. > 1GHz). A remedy is to process the signals at a lower rate in a parallel manner. While the polyphase approach i) applying one-step sample rate alteration (down/up-sampling) inherently operates in parallel, the hierarchical approach ii) being based on stepwise sample rate alteration calls for the parallelisation of, at least, the high rate stages.

In this contribution, the systematic sample-by-sample processing procedure for parallelisation of multirate systems by Groth is recalled. It is applied to the parallelisation of a novel class of tree-structured filter banks: The various steps towards parallelisation of the high rate front end of the FDM-demultiplexer part of the filter bank are described in detail.

I. INTRODUCTION

Digital signal processing on-board communication satellites (OBP) is an active field of research where, in conjunction with frequency division multiplex (FDMA) systems, presently two trends and challenges are observed, respectively: i) The need of an ever-increasing number of user channels makes it necessary to digitally process, i.e. to demultiplex, cross-connect and remultiplex, ultra-wideband FDM signals requiring high end sampling rates that range considerably beyond 1GHz [1], [2], [3], [4], [5], and ii) the desire of flexibility with channel bandwidth-to-user assignment calling for simply reconfigurable OBP systems [6], [7], [8], [9]. Yet, overall power consumption must be minimum demanding highly efficient filter banks for FDM demultiplexing (FDMUX) and remultiplexing (FMUX).

Two baseline approaches to most efficient uniform digital filter banks (FB), as required for OBP, are known: a) The complex-modulated (DFT PP) FB [10], and b) the multistage tree-structured FB, where its universal directional filter cells (UNDIFICE) are likewise based on the DFT PP method [11], [12]. For both approaches it has been shown that bandwidth-to-user assignment is feasible within reasonable constraints [7], [8], [13]: A minimum user channel bandwidth, denoted by slot bandwidth \(b\), can stepwise be extended by any integer number of additional slots up to a desired maximum overall bandwidth that shall be assigned to a single user.

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However, as to challenge i), the above two FB approaches fundamentally differ from each other: In a DFT PP FDMUX (a) the overall sample rate reduction is performed in compliance with the number of user channels in a single step: all arithmetic operations are carried out at the (lowest) output sampling rate [10]. In contrast, in the multistage FDMUX (b) the sampling rate is reduced stepwise, in each stage by a factor of two [11]. As a result, the polyphase approach (a) inherently represents a completely parallelised structure, immediately usable for extremely high front end sampling frequencies, whereas the high end stages of the tree-structured FDMUX (b) cannot be implemented with standard space-proved CMOS technology. Hence, the tree structure, FDMUX as well as FMUX, calls for a parallelisation of the high rate stages.

As motivated, this contribution deals with the parallelisation of multistage multirate systems. To this end, we introduce a general systematic procedure for multirate system parallelisation [14], which is deployed in detail in Section II. For proper understanding, in Section III this procedure is applied to the high rate front end stages of the FDMUX part of the recently proposed tree-structured SBC-FDMUX FB [9], [13], which uniformly demultiplexes an FDM signal always down to slot level (of bandwidth \(b\)) and that, after on-board switching, recombinates these independent slot signals to an FDM signal (FMUX) with different channel allocation – FDMUX functionality. If a single user occupies a multiple slot channel, the corresponding parts of FDMUX and FMUX are matched for (nearly) perfect reconstruction of this wideband channel signal – SBC functionality [10]. Finally, some conclusions are drawn to stimulate further research.

II. SAMPLE-BY-SAMPLE APPROACH TO PARALLELISATION

In this section, we introduce the novel sample-by-sample processing (SBSP) approach to parallelisation of digital multirate systems [14] where, without any additional delay, all incoming signal samples are directly fed into assigned units for immediate signal processing. Hence, in contrast to the widely used block processing (BP) approach, SBSP does not increase latency.

In order to systematically parallelise a (multirate) system, we distinguish four procedural steps [14]:

1. **Partition the original system** in (elementary SISO or MIMO) subsystems \(E(z)\) with single or multiple input and/or output ports, respectively, that are simply amenable to parallelisation. To enumerate some of these: Delay, multiplier, down- and up-sampler, summation and branching, but also
suitable compound subsystems such as SISO filters and FFT transform blocks.

2. **Parallelise each subsystem** $E(z)$ in an SBSP manner according to the desired degree of parallelisation $P$. To this end, each subsystem is cascaded with a $P$-fold SBSP serial-to-parallel (SP) commutator for signal decomposition (demultiplexing) followed by a consistently connected $P$-fold parallel-to-serial (PS) commutator for recomposition (remultiplexing) of the original signal, as depicted in Fig. 1(a). Here, obviously $P = P_{SP} = P_{PS}$, and $p \in [0, P - 1]$ denotes the relative time offsets of connected pairs of down- and up-samplers, respectively. Evidently, the $P$ output signals of the SP interface comprise all polyphase components of its input signal in a time-interleaved (SBSP) manner at a $P$-fold lower sampling rate [10], [12]. Since the subsequent PS interface is inverse to the preceding SP interface [12], the SP-PS commutator cascade has unity transfer with zero delay in contrast to the $(P - 1)$-fold delay of the BP Delay-Chain Perfect-Reconstruction system [10], as anticipated (cf. also Fig. 2).

After this preparation, $P$-fold parallelisation is readily achieved by shifting the (SISO) subsystem $E(z)$ between the SP and PS interfaces by exploiting the noble identities [10] and some novel generalised multirate identities [14], [15]. Thus, as shown in Fig. 1(b), the two interfaces are interconnected by an equivalent $P \times P$ MIMO system $E(z)$, which represents the $P$-fold parallelisation of $E(z)$, where all operations of which are performed at a $P$-fold reduced operational rate.

3. **Reconnect all parallelised subsystems** exactly in the same manner as in the original system. This is always given, since parallelisation does not change the original numbers of input and output ports of SISO or MIMO subsystems, respectively.

4. **Eliminate all interfractional cascades of PS-SP interfaces** using the obvious multirate identity depicted in Fig. 2. Note that this elimination process requires identical up- and down-sampling factors, $P_{out}^{ab} = P_{in}^{h}$, of each PS-SP interface cascade restricting free choice of $P$ for subsystem parallelisation. As a result of parallelisation, all input signals of the original (possibly MIMO) system are decomposed into $P$ time-interleaved polyphase components by a SP demultiplexer for subsequent parallel processing at a $P$-fold lower rate, and all system output ports are provided with a PS commutator to interleave all low rate sub-signals to form the high speed output signals.

For illustration, we present the parallelisation of a unit delay $z^{-1} := z_{s}^{-1/P}$, and of an $M$-fold down-sampler with zero time offset ($p = 0$)
decimation by two, the PP branch filters branching and blocking (delay 300MHz all subsystems preceding the third stage down to front end parallelisation has to reduce operational clock of deemed feasible using present-day CMOS technology. Hence, allocation scheme [13];

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 z^{-1} \text{ is parallelised by } P_0 = 8, \text{ as shown in Fig. 3(a), while the subsequent down-sampler applies } P_1 = 4, \text{ as described above w.r.t. Fig. 3(b). Immediate cascading of parallelised unit delay } (P_0 = 8) \text{ and down-sampling } (P_1 = 4, M = 2) \text{ (as induced by Fig. 3) shows that only those four PP components of the parallelised delay with even time offset } (p = 0, 2, 4, 6) \text{ are transferred via the 4-branch SP-input interface of down-sampling } (2P_1 = 8) \text{ to its PS-output interface with naturally ordered time offsets } p = 0, 1, 2, 3 \text{ w.r.t. } P_1 = 4. \text{ Hence, only those retained 4 out of 8 PP components of odd time index } p = 7, 1, 3, 5, \text{ being provided by the unit delay’s SP-input interface and delayed by } z^{-1} = z_{e1}^{-1}, \text{ are transferred (mapped) to the } P_1 = 4 \text{ up-samplers with timing offset } p = 0, 1, 2, 3 \text{ of the 4-branch PS-output interface of the down-sampler. Fig. 5 shows the correspondingly rearranged signal flow graph representation of stage 1 input section } (\nu = \lambda = 1).

As a result, the upper branch of stage 1, \( H_0(z_{\nu}) \rightarrow H_1^{\nu}(z_{\nu}) \), is fed by the even-indexed PP components of the high rate FDMUX input signal, whereas the lower branch \( H_1(z_{\nu}) \rightarrow H_1^{\nu}(z_{\nu}) \) is provided with the delayed versions of the PP components of odd index, as depicted in Fig. 5. Hence, as in the original system Fig. 4, the input sequence is completely fed into the parallelised system.

This procedure is repeated with the input branching and blocking sections of subsequent stages \( \nu = 2, 3 \). The PP branch filters \( H_0(z_{\nu}) \rightarrow H_1^{\nu}(z_{\nu}) \) parallelised by \( P_0 \), where \( P_2 = 2 \) and \( P_3 = 1 \) \( (P_1 = 4), \) are provided with the even-numbered PP components of the respective input signals with timing offsets in natural order. Contrary, the set of PP components of odd index is always delayed by \( z_{e1}^{-1}/P_{\nu-1} \) and fed into filter blocks \( H_1(z_{\nu}) \rightarrow H_1^{\nu}(z_{\nu}) \) in crossed manner (cf. input section \( \lambda = 1 \)).

3. \( P_{\nu} \)-fold Parallelisation of PP branch filters \( H_\lambda(z_{\nu}) \rightarrow H_\lambda^{\nu}(z_{\nu}), \lambda = 0, 1; \nu = 1, 2, 3, \) is achieved by systematic application of the procedure condensed in Fig. 1 (for details cf. [14], [12]). To this end, \( H_\lambda(z_{\nu}) \) is decomposed in \( P_{\nu} \) PP components of correspondingly reduced order, which are arranged to a MIMO system by exploiting a multitude of multirate identities [14], [15]. The resulting \( P_{\nu} \times P_{\nu} \) MIMO filter transfer matrix \( H_\lambda^{\nu}(z_{\nu}) \) contains each PP component of \( H_\lambda(z_{\nu}) \) \( P_{\nu} \) times: Thus, the amount of hardware is increased \( P_{\nu} \) times whereas, as desired for feasibility, the operational clock rate is concurrently reduced by \( P_{\nu}. \) Hence, the overall expenditure, i.e. the number of operations times the respective operational clock rate [12], is not changed.

4. Parallelisation of butterflies combining the output signals of associated PP filter blocks is straightforward: For each (time-interleaved) PP component of the respective signals a butterfly has to be foreseen, as shown in Fig. 5.

IV. CONCLUSION

A general and systematic procedure for parallelisation of multirate systems has been presented. Its application to the high rate decimating FDMUX front end of the tree-structured SBC-FDFMUX FB [9], [13] has been deployed in detail. The stage \( \nu \) degree of parallelisation \( P_{\nu}, \nu = 0, 1, 2, 3, \) is
diminished proportionally to the operational clock frequency $f_\nu$ of stage $\nu$ and is, thus, adapted to the actual sampling rate. As a result, after suitable decomposition of the high rate front end input signal by an input commutator in $P_0 = P_{\text{max}}$ polyphase components (as depicted for $P_{\text{max}} = 8$ in Fig. 5), all subsequent processing units are likewise operated at the same operational clock rate $f_s = f_1 / P_0$. Since inherent parallelism of the original tree-structured FDMUX (Fig. 4) has attained $P_{\text{max}} = 8$ in the third stage, and the output signals of this stage represent the desired eight demultiplexed FDM subsignals, interleaving PS-output commutators are no longer required, as to be seen in Fig. 5. Finally, it should be noted that parallelisation does not change overall expenditure; yet, by multiplying stage $\nu$ hardware by $P_\nu$, the operational clock rates are reduced by a factor of $P_\nu$ to a feasible order of magnitude, as desired.

Applying the rules of multirate transposition [12] to the parallelised FDMUX front end, the high rate interpolating back end of the tree-structured SBC-FDMUX FB is obtained likewise and exhibits the same properties as to expenditure and feasibility [14]. Hence, the versatile and efficient tree-structured filter bank (FDMUX, FMUX, SBC, wavelet, or any combination thereof) can be used in any (ultra) wide-band application without any restriction.

REFERENCES


