HIGH THROUGHPUT BENT-PIPE PROCESSOR FOR FUTURE BROADBAND SATELLITE ACCESS NETWORKS

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1 INTRODUCTION

The competitiveness of the satellite in access communication systems is today more and more threatened by the considerable continuous progress seen in terrestrial fixed and wireless communications networks. Nevertheless satellites still represent an attractive solution for broadcasting, multicasting and point-to-point communications, because of their coverage capability, limited ground infrastructure required and flexibility. In order to enhance the position of the satellite in the future communication systems market, a further step is needed to increase the on-board available capacity and flexibility of the payload.

Within the perspective of the “Next Generation of Broadband Multimedia Satellite Systems”[11] extremely high rate gateway links in Q-band serving hundreds of Ka-band user beams through a high throughput and highly flexible satellite processor seem to be very attractive in order to boost the satellite system capacity. This should significantly reduce the cost of satellite access for the end-user due to an increased throughput and enhanced flexibility in terms of connectivity.

This next generation of satellite communication systems for access networks asks for requirements such as very high throughput processors, with enhanced flexibility in terms of channel bandwidth and connectivity, and processing of high number of user beams. Indeed, an efficient exploitation of available limited spectrum resources requires the implementation of large frequency re-use among the user beams and the flexibility in bandwidth, beam shaping and power transmission associated to each channel. Recently, the Agency has conducted pioneering research studies on transparent processors for satellite broadband access networks, during which several payload architectures and specific functionalities were investigated in order to support the stringent requirements brought by the next generation of broadband satellite communication systems.

This paper presents possible payload and processor architectures responding to the requirements of the next generation of broadband access networks via satellite, targeting throughputs higher than 50 Gbps.

First the access system scenario is described, i.e. frequency planning, physical layer, access method. The payload requirements in terms of processed bandwidth, connectivity, flexibility in channel sizing, beam forming and power allocation are derived from the system requirements. In a second step, two generic classes of processor architectures are differentiated: beam port architectures and feed port architectures. Based on this classification different payload/processor architectures that support the baseline system requirements are described. The present paper only tackles the forward link as it is expected to be the most limiting one. In a third step, the different signal processing algorithms of the processor are presented: demultiplexing, switching, beam forming and analogue to digital conversion. These algorithms will be used as models to assess the complexity of the different processor architectures to be traded off, taking also into account their flexibility and scalability. Finally preliminary satellite system capacity estimation is provided for the different payload architectures.

2 THE BROADBAND SATELLITE ACCESS SCENARIO

The scenario considered for this processor study is called the “distributed access network” scenario and is depicted on Fig. 1 (a). It is supposed to provide high capacity point-to-point and multicasting services for ubiquitous Internet access. The assumed network topology is multi-star with a few gateways providing ground network access points (IXP) to a
very large community of small users. On the user link side narrow unicast beams and broadcasting beams are simulta-
neously present. User terminals aggregate just one or few users so that an unbalanced traffic is generated. Because the
application described requires the individual access to the core (Internet) network, there is no requirement for on board
demodulation and routing. We then assume transparent satellite payload architecture with asymmetric forward and reverse links.

2.1 General Overview

![Fig. 1](image) (a) Satellite Distributed Access Scenario. (b) Baseline System Requirements.

Forward Link Description

On the Forward link, a total processed useful bandwidth of 36 GHz is envisaged, served by 9 gateway beams. One ac-
tive gateway per beam is assumed, other gateways being used in site diversity configuration. The gateway uplink is in Q
band (47.2 – 49.7 GHz) and a 2.5 GHz bandwidth (around 2 GHz useful) is allocated to each beam. A full frequency re-
use pattern in both polarizations is assumed, provided that the beam locations are far enough one from each other to
limit the generated interference. Each gateway transmits a multi-carrier stream (MF/TDM) to address a given number of
user beams with one carrier per beam.

The downlink is in Ka band and each user beam can be allocated in average around 166 MHz in a 1:3 frequency re-use
scheme, giving a total bandwidth reservation of around 500 MHz (e.g. 18.8 – 19.3 GHz). As explained further in this
section, the connectivity requirements imply that each user beam is able to receive simultaneously TDM from several
gateways; therefore a MF/TDMA stream is needed to support the downlink traffic.

The total processed bandwidth on the forward uplink is given by: 2 GHz x 2 x 9 = 36 GHz and is fully supported by the
downlink (i.e. 216 x 166 MHz).

Return Link Description

On the Return link, the total processed bandwidth of 10.8 GHz is considered. The uplink is in Ka band and each user
beam is allocated a 50 MHz bandwidth. A frequency re-use pattern of 1/3 is assumed, giving a total bandwidth of 150
MHz (bandwidth reservation around 200 MHz e.g. 28.2 – 28.4 GHz). Users inside the beam can access to the satellite in
a MF/TDMA fashion. In order to satisfy the connectivity requirements, the users inside the beam shall be able to trans-
mitt together to different gateway beams.

The downlink is in Q band and each gateway beam is allocated a 600 MHz (e.g. 41.0 – 41.6 GHz) bandwidth in both
polarizations, giving a total beam bandwidth around 1.2 GHz. A full frequency re-use pattern in both polarizations is
assumed and each gateway beam receives an MF/TDM stream.
The dissymmetry between the Forward and the Return links is actually linked to the Internet traffic that usually consists in large forward traffic against small requests from the user.

2.2 System Flexibility Requirements

Within the frame of the Next Generation Broadband Satellite Systems, new flexibility areas have been identified for these future access scenarios where the traffic is likely to be varying and non-uniform in order to optimize this total capacity: flexibility in power to beam allocation, flexibility in bandwidth to beam allocation, flexibility in feeder link channel to beam connectivity and advanced beam forming capabilities (flexibility in beam shaping, beam hopping...). Increased capacity and flexibility are indeed the major factors likely to reduce the cost of satellite services and therefore bring strong confidence to the operators of the viability of such systems. The following sub-sections describe briefly these flexibility requirements for the forward link.

Bandwidth to beam allocation and granularity requirements

As a baseline, a 1:3 frequency re-use scheme has been considered leading to an average bandwidth around 166 MHz per user beam. However, in order to cope with traffic non-uniformity between the different beams, the system should be able to re-allocate to a beam the unused bandwidth with a granularity of 10 MHz (12 MHz channel spacing). This granularity is also the one used to introduce flexibility on the TDMs bandwidth with steps of 12 MHz, using the contiguous filtering property (allows recombination of channels).

Therefore assuming a total bandwidth of 504 MHz on the user link (i.e. 42 channels of 12 MHz), 14 channels per beam can be used on average for a full MF/TDM downlink if a frequency re-use of 3 is assumed (168 MHz useful bandwidth on average per beam). This channel-based decomposition of the spectrum should also allow allocating to a beam any bandwidth within the interval [0…168 MHz] with a granularity of 12 MHz. However, the maximum TDM size inside a MF/TDM downlink beam shall still be limited to 120 MHz (10 basic channels) in order not to jeopardize too much the link budget and limit the complexity of the receiver. The general representation of the signal is depicted on Fig. 2.

The number of channels is thus equal to 3024 (i.e. 216 x 14) and is fully supported by the gateway side, 168 channels per polarization per gateway beam being assumed (2,016 GHz/Polarization/Gateway).

Connectivity Requirements

As far as the connectivity between the gateway beams and the user beams is concerned, a user beam can be connected to several gateway beams in both forward and return links. This implies that a MF/TDM stream is used on the forward downlink as depicted on Fig. 3. This connectivity scenario corresponds to the case where different NAPs may provide access to the same coverage area. This is the most likely scenario since it is expected that a system of such high capacity involve several NAPs. From a processor impact point of view, this potentially has a very strong effect. Indeed if the reference model was oriented towards one extreme rigid case of “one user beam – one gateway scheme”, with each gateway dealing with a set number of user beams, one could start questioning the need for a processor.
In order to cope efficiently with the non-uniformity of the traffic inside the different user beams, a power to beam allo-
cation flexibility of $-10 \text{ dB to } +3 \text{ dB}$ around the average nominal power shall be achieved.

**Table 1** summarizes the requirements to fulfill in the design of suitable payload and processor architecture for the for-
ward link.

<table>
<thead>
<tr>
<th><strong>Baseline System Requirements – Forward Payload</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Uplink Band</strong></td>
<td>47.2 – 49.7 GHz</td>
</tr>
<tr>
<td><strong>Downlink Band</strong></td>
<td>18.8 – 19.3 GHz</td>
</tr>
<tr>
<td><strong>Baseline Frequency reuse pattern on user side</strong></td>
<td>1/3</td>
</tr>
<tr>
<td><strong>Frequency reuse pattern on gateway side</strong></td>
<td>Full</td>
</tr>
<tr>
<td><strong>Average bandwidth/ user beam</strong></td>
<td>168 MHz</td>
</tr>
<tr>
<td><strong>Bandwidth to beam allocation flexibility</strong></td>
<td>0 – 168 MHz</td>
</tr>
<tr>
<td><strong>Granularity</strong></td>
<td>10 MHz (12 MHz spacing)</td>
</tr>
<tr>
<td><strong>Maximum TDM bandwidth</strong></td>
<td>120 MHz</td>
</tr>
<tr>
<td><strong>Bandwidth/ GW beam</strong></td>
<td>2.5 GHz x 2 (Both polarizations)</td>
</tr>
<tr>
<td><strong>Total processed bandwidth</strong></td>
<td>40 GHz</td>
</tr>
<tr>
<td><strong>Equivalent useful bandwidth</strong></td>
<td>36 GHz</td>
</tr>
<tr>
<td><strong>Uplink Access</strong></td>
<td>MF/TDM</td>
</tr>
<tr>
<td><strong>Downlink Access</strong></td>
<td>MF/TDM</td>
</tr>
</tbody>
</table>

### 3 GENERAL METHODOLOGY

This paper focuses on the forward link as it is considered to be the most demanding. In order to assess the forward link
capacity of the system, the available RF power at the antenna needs to be determined. The DC power limitation is given
by the platform capabilities – 18 kW available DC power considering the current AlphaBus limitations. Taking into
account the system requirements in terms of bandwidth, flexibility, connectivity, number of beams… a preliminary es-
timation of the processor power consumption can be derived from its architecture and the algorithms implemented in
the different functional blocks. Once the DC power consumption of the digital processor and payload is known, the
goal is to maximize the available RF power delivered by the TWTAs (depending on the flexibility requirements) on the
transmit side in order to maximize the system capacity, the latter being determined by the available RF power per beam
and the antenna beam pattern. The methodology followed in this study is depicted on Fig. 4. The paper aims at achiev-
ing a full first iteration of the iterative process.
4 PROCESSOR ARCHITECTURES

The following sections present the different processor architectures. The classification is based on the processor architectures:

- **The beam port architectures**: in these architectures each active signal port of the digital processor is linked uniquely to a specific beam. These architectures include:
  i. The single feed/beam design in which a set of array fed reflectors is used to illuminate the coverage area with a set of spot beams. Each spot is generated by a single feed.
  ii. An architecture based on semi-focussed reflector geometry with analogue beamforming. The number of inputs / outputs on the processor side of the beamformer corresponds to the number of beams with those on the antenna side corresponding to the number of feeds

- **The feed port architectures**: these architectures incorporate digital beam forming (DBFN) within the processor. A critical factor in this architecture is the required amplitude and phase matching which has to be maintained all the way from the DSP outputs up to the antenna feed array, and includes the matching within the multiport amplifier scheme. These architectures concern essentially the following antenna subsystems:
  i. Semi-focussed reflector
  ii. DRA: not considered here

4.1 Beam Port Architectures

[Fig. 5] depicts the general beam port architecture, interfacing at IF level with the remaining part of the payload. The incoming feeder signals, coming out from the Anti-Aliasing Filter (AAF) are sampled at 2.4 Gsps (real sampling) and quantised with nominally 8 bits (see Fig. 5). The sampled signal is feeding a demultiplexing device that generates 84 useful channels of 12 MHz (10 MHz useful bandwidth per individual channel) and performs simultaneously the real to complex conversion of the signal. A 3024 x 3024 switch matrix allows flexible mapping of any frequency uplink channel towards any beam and frequency downlink channel. Flexible power per beam allocation can be achieved through the level control stage. Finally a multiplexing operation of the entire set of channel slots is performed for each element before digital to analogue conversion at 400 Msp.
4.2 Feed Port Architecture

Fig. 7 depicts the general feed port architecture, interfacing at IF level with the remaining part of the payload. The incoming feeder signals, coming out from the Anti-Aliasing Filter (AAF) are sampled at 2.4 Gsps (real sampling) and quantised with 8 bits. The sampled signal is feeding a demultiplexing device that generates 84 channels of 10 MHz (12 MHz useful bandwidth) and performs simultaneously the real to complex conversion of the signal. A 3024 x 3024 switch matrix allows flexible mapping of any frequency uplink channel towards any frequency downlink channel. The channels are thus gathered into groups of frequency re-use channels (channels that will re-use the same frequency on the user coverage). Inside the digital beam forming function, a weighting of the channels with regards to the different feeds is performed as well as a frequency re-use concentration between all the channels sharing the same feed (as they are on the same frequency slot). In that sense, the beam forming operation performs a routing operation for the particular channel. Finally a multiplexing operation of the entire set of channel slots is performed for each element before analogue to digital conversion at 1.2 Gsps.

Though the power consumption of this architecture is likely to be higher than for the beam port architecture, the digital beam forming architecture (also called feed port architecture) presents several advantages in terms of flexibility. Indeed, the digital beam forming allows full beam shaping and pointing flexibility, but also increase the flexibility in terms of bandwidth to beam allocation since the full bandwidth of 504 MHz can now be routed to any beam.
5 PROCESSOR SUBSYSTEMS COMPLEXITY AND DEGRADATION ESTIMATION

A detailed description of a slightly modified processor approach is given in [4].

5.1 Analogue to Digital and Digital to Analogue Conversion

ADC and DAC Characteristics

ADC working at the required very high sampling frequency is only emerging. Poulton and al. ADC 4-Gsps, 6-bits (ENOB = 5.2), with 1.8-GHz input available bandwidth is among the one offering sampling rate of 2.4 Gsps minimum. Some of its characteristics are summarized in [4]. In fact, the total power consumption due the analogue to digital conversion is not only determined by the converter itself, but also by the serial-to-parallel demultiplexer placed at the output of the converter in order to decrease the data rate to CMOS compatible values. Therefore, to the 5.7 Watts power consumption of the ADC, one has to add around 4 Watts for the demultiplexer, yielding to a total power consumption of the signal conversion stage inside the processor of $36 \times 9.7 \text{ W} = 349.3 \text{Watts}$.

As far as the digital to analogue converters are concerned, the feed port architecture requires the use of high-speed ADC at 1.2 Gsps. The ATMEL TS86101G2 device offers a 10-bits (8 bits effective), 1.2 Gsps DAC, and consumes around 3.0 Watts (including the multiplexer at the input of the DAC). This leads to an overall power consumption of the digital to analogue conversion stage of $768 \text{ Watts} (256 \times 3 \text{ Watts})$ for the feed port architecture. The beam port architecture has less stringent requirements in terms of conversion speed and a 2.0-Watts DAC can be considered, yielding to a total power consumption of $216 \times 2 = 432 \text{ Watts}$.

ADC and DAC output signal

The theoretical performance of an ideal ADC with a Gaussian input signal is well documented. There is an optimum drive point which maximizes the S/N and results from a trade-off between the quantisation noise and the clipping noise. Fig. 8(a) illustrates this trade-off for a 5.2 ENOB ADC; the optimum peak factor for scaling depends on the effective number of bits (ENOB) and is equal to 3 in this case. This means that the input signal power has to lie around –10dB below the full scale ADC dynamic. Fig. 8(b) represents the degradation of the ADC versus the feeder bandwidth for an infinite input SNR, taking into account the clock and aperture jitter, the gain error and DC offset in addition to the classical quantisation and clipping effects. The worst-case degradation read from Fig. 8(b) corresponds to an $\text{SNR}_Y$ of 24.9 dB being exclusively caused by the ADC provided that $\text{SNR}_X = \infty$. Note that an ideal ADC with ENOB = 5.2 bit yields $\text{SNR}_Y = 33 \text{ dB}$. A detailed analysis of the ADC degradation modeling is presented in [4].
As far as the DAC is concerned, the ATMEL TS86101G2 can provide a minimum of 8 effective bits. Applying a similar analysis as for the ADC, this leads to an overall $\text{SNR}_Y$ for the stage of 40.6 dB. Note that the ideal DAC with ENOB = 8 yields to $\text{SNR}_Y = 49.9$ dB.

![Graph](image)

(2) $\text{SNDR}_Y$ for ENOB=5.2 with quantisation and clipping errors. (b) Overall $\text{SNR}$ degradation inside the different channels for an input $\text{SNR}_{X=\infty}$.

### 5.2 Frequency Demultiplexing/Multiplexing

**Demultiplexer Description**

Fig. 9 depicts the two-stage structure of the demultiplexer (For a detailed description refer to [2],[4]). Every channel is assigned to an output. The first stage (Coarse FDMUX) consists of a 20-channel polyphase FFT filter bank that performs inherently the transition from real to complex signal processing. Only 10 of the 20 output signals are useful for further demultiplexing, whilst the other 10 output signals are discarded. Since each output signal comprises 10 granules of 12 MHz, flexibility in channel sizing is guaranteed. The structures of the different tree-modules (Fine FDMUX) are shown in Fig. 9(b). The system depicted in Fig. 9(b) represents the tree-modules of Fig. 9(a). The tree-module2 comprises the stages 2a, 2b, 2c and 3 for demultiplexing of FDM signals with all slots used. The tree-module1 and the tree-module3 can be derived from tree-module2 by canceling all processing foreseen for unused slots, since the channels with the index from 0 to 7 and from 92 to 99 are idle. Hence, the tree-module 2 can be modified correspondingly to reduce the computational load. As a result, the tree-module1 for demultiplexing the channels 8 and 9 comprises only stage 2a and the elements in Fig. 9(b) highlighted in dark-gray, while the tree-module3 for demultiplexing the channels 90 and 91 comprises the stage 2a and the elements of Fig. 9(b) highlighted in light gray.

| Table 2 below contains the information on the prototype filters, which are applied in the different stages: | | |
|---|---|---|---|---|---|
| **PP-FFT-FB** | **Tree** | **BF** | **Comments** |
| Stage | 1 | 2a, 2b, 2c, 3 |
| Filter Type | Lowpass, Halfband, Halfband, Halfband |
| $f_c$/MHz | 2400, 240, 120, 60, 30 |
| $M$ | 10 / 2 |
| $N$ | 59 / 11 |
| $N_{eff}$ | 59 / 11 |
| $G$ | 1 / 10 |

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**Overall Power Consumption**

Power consumption is essentially governed by the multiplication rate of the system, i.e. the overall number of multiplications times the corresponding operational rate $f_{op}$. The overall multiplication rate is determined by appointing the multiplications of the several stages of the demultiplexer. The latter consists of four classes of multipliers to be weighted by the respective clocks:

- the number of multiplications due to filtering: $N_{eff}$,
- the number of multiplications $A_{OCA}$ due to the additionally needed $2M-1$ modulations (half-complex multiplications) because of the odd channel allocation scheme,
- the number of complex multiplications of the FFT computation: $N_{FFT} \cdot \log_2(N_{FFT})$
- the number of multiplications $A_{ISP}$ of additional $M/2$ modulations allowing for an identical signal processing. $A_{ISP}$ can be neglected since these modulations can be realized by simple sign manipulation.

The third stage differs from the two first stages since $A_{OCA}$, $A_{FFT}$ and $A_{ISP}$ equal zero. Instead of that the modulations to center the respective channel at zero frequency has to be considered by $A_{CC}$. The total multiplication rate is given by:

$$A = \sum_{i=1}^{3} (A_{\text{FILT},i} + A_{\text{OCA},i} + A_{\text{FFT},i}) + N_{\text{addMod}} \cdot A_{\text{CC,3}}$$

Where $N_{\text{addMod}}$ represents the number of bandlimiting filters needing an additional modulation.

The overall multiplication rate has been estimated to $158265 \times 10^6$ multiplications per second. Considering an ASIC operating at $f_{op} = 100 \text{ MHz}$, the total number of multipliers required is given by:

$$N_{\text{multiplier}} = \frac{A}{f_{op}} = 1583$$

Considering 1200 gates for an 8x8 multiplier, the total number of gates required for the demultiplexer is around 1.9 Mgates, which is well below current ASIC limitations (8 Mgates). Therefore 10 ASICs could be sufficient, in a first approximation, to implement the set of 36 wideband demultiplexers. The power consumption of one demultiplexer can be computed on the basis of the ATMEL18-RHA 0.18 $\mu$m process (0.01μW/gate/MHz):
This results in a total power consumption of 72 W. Allowing for a 20% margin for addition and memory will raise the power consumption to roughly 86 Watts.

### SNR degradation

Assuming a power level of $S=1$ and no noise in front of the demultiplexer, the SNR at the output of the coarse FDMUX results in

\[
\text{SNR}_{CD} = 10 \cdot \log_{10} \left( \frac{1}{9 \cdot 10^{-9/10}} \right)
\]

since, due to downsampling, $M-1 = 9$ aliasing components are spectrally folded onto the usable channels; $a_c$ represents the stopband attenuation common to all filters involved (50 dB). In the following stages of fine FDMUX altogether four additional aliasing components are spectrally folded onto the usable channels leading to an SNR at the output of the demultiplexer of:

\[
\text{SNR}_{\text{output}} = 10 \cdot \log_{10} \left( \frac{1}{(9+4) \cdot 10^{-9/10}} \right) = 38.8 \text{ dB}
\]

where $a_c = 50$ dB is assumed [4].

### Multiplexer Description

As far as the multiplexing operation on the user side is concerned, a similar architecture as the one developed for the demultiplexer results by applying the transposition theorem [3]. The main difference will reside in the first stage (polyphase filter) due to the limitation of the total number of useful channels 14 and 42 instead of 84 for the beam architecture and feed port architecture respectively. The overall multiplication rate is thus reduced to $37841 \times 10^6$ multiplications per second for the beam port architecture, leading to a total power consumption of 0.5 Watt per multiplexer. In the case of the feed port architecture, the multiplication rate is reduced to $88447 \times 10^6$ multiplications per second, giving a total power consumption of 1.1 Watts per multiplexer.

The overall power consumption of the multiplexing stage will therefore be equal to 130 Watts and 338 Watts for the beam port architecture (216 multiplexers needed) and for the feed port architecture (256 multiplexers needed) respectively, taking into account a 20% margin for the additions and memory power consumption. This drastic increase in power consumption of the feed port architecture multiplexer stage with regards to the beam port architecture is mainly due to the increased bandwidth to be multiplexed (504 MHz), which implies that the full 500 MHz bandwidth is potentially available on each beam. This is one of the costs to pay for the flexibility provided by the digital beam forming architecture.

### 5.3 Wideband Digital Beam Forming

The processor architectures discussed in section 5.1 and 5.2 divide between those that interface with the processor on the user link side on a beam port basis and on a feed/element port basis; digital beam forming is only relevant in the latter case. Depending on the applications and precise requirements, many different digital beamforming architectures can be designed and optimized. The objective of this paper being more focused on the full processor/payload, we only present here a simple DBFN architecture based on a switch matrix and a set of multipliers and adders. The input channels are frequency re-use channels, i.e. channels that use the same frequency slot on different beams of the coverage. It is assumed that a maximum of 16 feeds/beam is necessary to produce the beams and that each beam can only form a maximum of 16 beams per channel. Therefore the architecture leads to a total of 1368 multipliers and 4096 adders working at 15 MHz. The resulting power consumption of the digital beam-forming network is equal to 1.1 Watt, yielding to a total DC power of the stage of 46.2 Watts (42 x 1.1 Watt). Fig. 10 depicts the DBFN architecture used for the determination of the digital processor power consumption.
5.4 Routing and Interconnection complexity

The candidate processor architectures include various switching functions and interconnecting function. Without going through the detailed implementation of these function, a preliminary estimation of the power consumption of these interconnection can be assessed, based on the estimation of the total flux of bits to be transferred between each stage. Seen the very high bandwidths to be processed, it is assumed that LVDS serial busses will be used to convey signals. If the HX3000 ASIC technology is considered, the power dissipation figures are around 0.07 Watts/Gbps. This yields to an overall power consumption of 300 Watts and 400 Watts for the beam port architecture and feed port architecture respectively.

5.5 Processor Architectures Summary

Global Signal to Noise Ratio

The degradation analysis is performed as follows. The gain of each processing subsystem is optimally adjusted so that the maximum signal level both at input and output are at the point, where the signal-to-noise ratio is maximum (cf. Fig. 8(a) for a peak factor of 3). Such a point exists which is a trade off between clipping when the signal is too high and reduced S/N as the signal is reduced. Typically, for a Gaussian signal, the optimum drive point is approximately 10 dB below the full-scale dynamic range (fsd) of the signal bus. Assuming a 1 Vpp ADC with a 50 Ω input resistance, the power level will thus be set to 13 dBm − 10 dB = -27dBW.

The noise introduced by the processor is caused by:

- Intermodulation in the IF stages.
- Quantization and clipping, non-linearity and jitter noise from the ADC and DAC.
- Adjacent channel interference. The SAW filter rejects such adjacent bands, the residual level being aliased back in band by sampling.
- Quantisation noise at each subsystem output. The output rms drive level with respect to fsd is assumed to be optimum. The quantisation noise is given by the theoretical value for digital stages.
- ACI due to aliasing and imperfect filtering in the channelising de-multiplexer and multiplexer.

The signal to noise ratio of the full processor can be computed via the following formula:
\[
\left( \frac{S}{N} \right)_{\text{processor}}^{-1} = \left( \frac{S}{N} \right)_{\text{ADC}}^{-1} + \left( \frac{S}{N} \right)_{\text{Demux}}^{-1} + \left( \frac{S}{N} \right)_{\text{DBFN}}^{-1} + \left( \frac{S}{N} \right)_{\text{Mux}}^{-1} + \left( \frac{S}{N} \right)_{\text{DAC}}^{-1}
\]

where the \( \text{SNR}_X = \infty \) is assumed in front of the processor.

Table 3 below summarizes the SNR of the different stages as well as the cumulative SNR.

<table>
<thead>
<tr>
<th>Stage</th>
<th>Bits</th>
<th>Quantization SNR [dB]</th>
<th>ACI SNR [dB]</th>
<th>Stage SNR [dB]</th>
<th>Cumulative SNR [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC [3]</td>
<td>5.2</td>
<td>33.0</td>
<td>47.0</td>
<td>24.9</td>
<td>24.9</td>
</tr>
<tr>
<td>DEMUX</td>
<td>8</td>
<td>49.9</td>
<td>38.8</td>
<td>38.5</td>
<td>24.7</td>
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<tr>
<td>DBFN</td>
<td>8</td>
<td>49.9</td>
<td>-</td>
<td>49.9</td>
<td>24.7</td>
</tr>
<tr>
<td>MUX</td>
<td>8</td>
<td>49.9</td>
<td>41.0</td>
<td>40.9</td>
<td>24.6</td>
</tr>
<tr>
<td>DAC</td>
<td>8</td>
<td>49.9</td>
<td>47.0</td>
<td>40.6</td>
<td>24.4</td>
</tr>
</tbody>
</table>

Table 3  Signal to Noise degradation Through The Digital Processor Stages

**Power Consumption Estimation**

Table 4 summarizes the main different contributions to the power consumption of the overall forward processor. Based on results given in Table 4 an estimate of the power consumption for the digital return processor has been derived and is shown in Table 5. The overall power consumption estimate for the processor is then given in Table 6 3000 Watts are needed for the feed port architecture while only 2000 Watts shall be sufficient for the beam port architecture.

<table>
<thead>
<tr>
<th>Stage</th>
<th>Beam Port Architecture</th>
<th>Feed Port Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>349</td>
<td>349</td>
</tr>
<tr>
<td>DEMUX</td>
<td>86</td>
<td>86</td>
</tr>
<tr>
<td>DBFN</td>
<td>0</td>
<td>46</td>
</tr>
<tr>
<td>MUX</td>
<td>130</td>
<td>338</td>
</tr>
<tr>
<td>DAC</td>
<td>432</td>
<td>768</td>
</tr>
<tr>
<td>Interconnect</td>
<td>320</td>
<td>430</td>
</tr>
<tr>
<td>Total</td>
<td>1317</td>
<td>2017</td>
</tr>
</tbody>
</table>

Table 4  Digital Forward Processor Power Consumption For the Beam Port and Feed Port Architectures

<table>
<thead>
<tr>
<th>Stage</th>
<th>Beam Port Architecture</th>
<th>Feed Port Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>324</td>
<td>512</td>
</tr>
<tr>
<td>DEMUX</td>
<td>50</td>
<td>150</td>
</tr>
<tr>
<td>DBFN</td>
<td>0</td>
<td>12</td>
</tr>
<tr>
<td>MUX</td>
<td>65</td>
<td>65</td>
</tr>
<tr>
<td>DAC</td>
<td>108</td>
<td>108</td>
</tr>
<tr>
<td>Interconnect</td>
<td>90</td>
<td>130</td>
</tr>
<tr>
<td>Total</td>
<td>637</td>
<td>977</td>
</tr>
</tbody>
</table>

Table 5  Digital Return Processor Power Consumption For the Beam Port and Feed Port Architectures

<table>
<thead>
<tr>
<th>Stage</th>
<th>Beam Port Architecture</th>
<th>Feed Port Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward link</td>
<td>1317</td>
<td>2017</td>
</tr>
<tr>
<td>Return link</td>
<td>637</td>
<td>977</td>
</tr>
<tr>
<td>Total</td>
<td>1954</td>
<td>2994</td>
</tr>
</tbody>
</table>

Table 6  Digital Processor Power Consumption Estimate For the Beam Port and Feed Port Architectures

6  PAYLOAD ARCHITECTURES

6.1  Antenna and Coverage Considerations

From a satellite orbital position of 9.2 degrees East, a Ka band coverage of Europe and North Africa with 216 beams on an hexagonal grid has been considered with a minimum edge of coverage gain of 50.5 dBi. A reflector size of 3.9 meters is required, assuming 65% efficiency reflector efficiency. Two cases have been considered:

---

1 The power consumption of the return processor is derived by a scaled-down operation based on the processed bandwidth and the granularity requirements. This is excluding the converters for which data have been taken from existing devices.
A Single Feed per Beam implementation using four reflectors on board. Four reflectors are required because the feed size would not allow the generation of adjacent beams from the same reflector. The total number of feeds required is obviously identical to the number of beam, i.e. 216, with around 54 beams per reflector antenna.

A Focal Array Reflector Antenna implementation using overlapping clusters of 7 feed per beam to generate the 216 beams from a single reflector. Using GRASP, the optimum amplitude and phase excitation for each feed was obtained in order to maximize the gain at beam center and minimize the gain on the directions of other beams using the same frequency assuming a three fold frequency reuse scheme. A total of 256 feed are required in this configuration.

Fig. 11 represents the 216 beams coverage, assuming a GEO satellite at 19.2 degrees longitude.

6.2 Transmit Forward Link Payload Architectures

Three different architectures have been considered for the transmit forward link:

6.2.1 Single Feed per beam payload architecture using “Flexible TWTAs”

This architecture, shown in Fig. 12 is of application for the case of antennas using single feed per beam. The main characteristics are the following:

- The digital processor provides 216 active beam port outputs each with a maximum of 170 MHz bandwidth, which corresponds to a 3-color frequency reuse scheme.
- 216 active up-converter/TWTA chains (one per beam) using 10:8 redundancy schemes.
- Up-conversion is implemented in two steps using two LO sources.
- Linearized “flexible” TWTA are used to provide in orbit flexible and efficient power to beam adjustment. The capability of controlling the TWT saturation power by control of anode voltage has been demonstrated recently.

The saturation power of the TWTA can be changed by 3 dB with only 2 to 3 points of percentage degradation in efficiency by controlling anode voltage and reoptimizing collector voltages for optimum efficiency. All TWTA in the payload are dimensioned for 3 dB higher saturation power than required for the average operational power per beam. Depending on traffic demand, the power of some beams can be increased by telecommand by up to 3 dB more, while other beams are simultaneously reduced in power in order to keep the limit on available DC power on board.
Different Output Back Off (OBO) conditions have been considered for the linearized TWTAs depending on the nature of traffic, i.e. 0.5 dB OBO for single TDM carrier per beam cases, 1.5 dB OBO for two TDM carriers per beam conditions and 3 dB OBO for multi-carrier per beam operation. The output losses have been estimated to 1.5 dB (composed of 0.2 dB for the isolator, 0.3 dB for the redundancy ring, 0.4 dB for the output filter and 0.6 dB waveguide runs). The TWTAs operate with an efficiency of 65% at saturation and 90% EPC efficiency.

6.2.2 **Multimatrix based architecture using analogue IF (or RF ) Beam Forming Network (BFN)**

This architecture, shown in Fig. 13, is of application for the case of Focal Array Feed Reflector antennas using overlapping clusters of feed. The main characteristics are the following:

- The digital processor provides 216 active beam port outputs each with a maximum of 170 MHz bandwidth, corresponding to a 3-colors frequency reuse scheme.
- Up-conversion is implemented in two steps using two LO sources.
- The Multilayer Beamforming Network (BFN) is implemented at IF. The BFN is used to generate 216 beams. The total number of feed outputs is 256. But the phase and amplitude control of only 7 feed is required for every beam.
- A multimatrix Tx RF front end is used, using high order (16x16) Ka band matrices. The multimatrix architecture allows for flexibility on power to beam allocation and beam pattern reshaping depending on traffic variations and maintaining at the same time a power efficient operation on board. High order matrices (16x16) are used, because of their high robustness to phase and amplitude errors that impact on beam isolation performance. Given the total number of feed (256), a total of 16 matrices are required. The implementation of beams using up to 16 feed each is therefore possible, for example for reduction of side lobe levels if required for the improvement of the downlink C/I within the coverage. A 20:16 redundancy scheme is considered within the different MPAs.
- An antenna using overlapping clusters of 7 feeds are used for every beam is assumed.

The linearized TWTAs used in the multimatrix configuration will have to operate under multi-carrier conditions with a significant power dynamic range, due to power to beam variations (+3 dB, -4 dB with respect to the uniform power per beam case) and to the feed excitation dynamics (estimated to be on the order of 6 to 7 dB). The TWTAs will operate with significant OBO (4 dB assumed); their efficiency is assumed to be 65% at saturation and 90% EPC. The output losses have been estimated to 2.3 dB (0.2 dB for the isolator, 0.3 dB for the redundancy ring, 0.8 dB for the waveguide runs, 0.6 dB for the output matrix and 0.4 dB for the output filter).

The main advantage of using an IF BFN instead of a digital BFN (see Section 6.2.3) resides in the fact that the digital processor can be built using a “beam port architecture”, providing 216 active outputs (instead of 256 in the case of a “feed port” implementation) and with reduced bandwidth (170 MHz instead of 500 MHz for the “feed port” case). This reduced bandwidth and number of ports allows drastic savings in power consumption for the digital processor: 3000 Watts have been estimated (forward and return processors) for a “feed port architecture” while only 2000 Watts are foreseen for the “beam port architecture”. This difference mainly comes from the reduction in the numbers of D/As and up-converters and from the large reduction of sampling rates of the D/A converters. Another advantage of the IF BFN is the absence of stringent phase and amplitude tracking requirements on the up-converter chains up to the BFN. An RF implementation would further reduce the number of up-converter chains and further relax tracking requirements; but the feasibility of large BFNs at 20 GHz, still need hardware demonstration.

6.2.3 **Multimatrix based architecture using digital BFN**

This architecture, depicted in Fig. 14, is similar to the concept presented before. The main difference is that the BFN functionality is included in the Digital Processor, leading to a “feed port processor” concept. The other main characteristics and assumptions given before remain also applicable in this case.

Although as mentioned before, this architecture implies a significant increase of power consumption on the digital processor (3000 Watts vs. 2000 Watts), it offers significant enhancements in terms of flexibility. In particular, it gives the possibility of implementing carrier to beam connectivity using the digital BFN functionality, an easier implementation of beam pattern reconfiguration and increased flexibility on bandwidth to beam assignment.
6.3 Estimation of available EIRP per beam

Considering the different payload architectures, a preliminary estimation has been made of the total available downlink RF power and the associated EIRP per beam.

The main assumptions are the following:

- The payload analysis approach described in Fig. 4 has been followed.
- 18000 Watts available on board payload DC power (Alpha Bus assumed).
- RF power to be transmitted on the return downlink (satellite to gateways) assumed to be around 10% of the transmitted power on the user downlink. This has been estimated assuming a factor four less overall transmitted bandwidth, a gateway G/T of 20 dB higher than the user terminals, similar on-board antenna gain, the difference of propagation losses (40 GHz vs. 20 GHz) and 6 dB difference in atmospheric losses, assuming gateway diversity is implemented.

The results obtained are synthesized in Table 7.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Total Downlink Rx RF power available</th>
<th>RF power per beam</th>
<th>EIRP/beam (Average on Coverage)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single feed per beam</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>with 1 TDM carrier / beam</td>
<td>4,23 kWatts</td>
<td>19,6 Watts</td>
<td>64,4 dBW</td>
</tr>
<tr>
<td>with 2 TDM carriers / beam</td>
<td>3,82 kWatts</td>
<td>17,7 Watts</td>
<td>64,0 dBW</td>
</tr>
<tr>
<td>With multicarrier/beam</td>
<td>3,24 kWatts</td>
<td>15,0 Watts</td>
<td>63,3 dBW</td>
</tr>
<tr>
<td>Multi Matrix Antenna</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>with analogue BFN</td>
<td>2,53 kWatts</td>
<td>11,7 Watts</td>
<td>62,2 dBW</td>
</tr>
<tr>
<td>with digital BFN</td>
<td>2,31 kWatts</td>
<td>10,7 Watts</td>
<td>61,8 dBW</td>
</tr>
</tbody>
</table>

Table 7 Power Budgets Summary of the Different Payload Architectures

Fig. 12. Single Feed per Beam Architecture – 216 beams, up to 170 MHz per feed (=beam)
IF1 | IF2 | Ka band (20 GHz)

Fig. 13. Multimatrix Architecture with Analogue Beam Forming Network – 216 beams, 7 feeds/beam, up to 170 MHz per beam

Fig. 14. Multimatrix Architecture with Digital Beam Forming Network – 216 beams, 7 feeds/beam, 500 MHz / feed
7 SATELLITE SYSTEM CAPACITY ESTIMATION

The overall system capacity has been estimated from the power budgets shown in Section 6.3. The capacity analysis is performed taking into account the use of Adaptive Coding and Modulation (ACM), which allows avoiding the system dimensioning for the worst case and benefiting from the C/I and fading location dependence. The DVB-S2 physical layer assumptions have been taken as a baseline for the set of codes and modulations to perform the simulations [6]. Detailed explanations and justifications on the applied methodology can be found in [5].

The following table gives a summary of the results obtained for the main architectures considered in this paper.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>RF power per beam</th>
<th>NPR</th>
<th>System Capacity</th>
<th>System Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Freq. Reuse = 3</td>
<td>Freq. Reuse = 4</td>
</tr>
<tr>
<td>Single feed per beam (Single Carrier)</td>
<td>12.4 dBW</td>
<td>/</td>
<td>73.0 Gbps</td>
<td>64.6 Gbps</td>
</tr>
<tr>
<td>MMA with analogue BFN</td>
<td>10.3 dBW</td>
<td>19 dB</td>
<td>65.9 Gbps</td>
<td>57.0 Gbps</td>
</tr>
<tr>
<td>MMA with digital BFN</td>
<td>10.0 dBW</td>
<td>18 dB</td>
<td>64.8 Gbps</td>
<td>55.3 Gbps</td>
</tr>
</tbody>
</table>

Table 8 RF power and system capacity estimates for proposed architectures

8 CONCLUSIONS

This paper has presented a full first iteration of a high-throughput payload dimensioning for future broadband access satellite networks. Mainly focused on the signal processing aspects, it presents a possible implementation of the processor functionalities, leading to two types of processor architectures: beam port and feed port architectures. The main interests of these two architectures have been compared together trading off important parameters such as overall power consumption, flexibility (in beam shaping and bandwidth to beam allocation) and their impact on the overall payload. The feed port architecture has been estimated to represent an increase of 1000 Watts more with regards to the beam port architecture (2000 Watts); it represents the cost to pay to increase the on-board processor flexibility (beam shaping, pointing, frequency to beam allocation).

Finally the capacity analysis performed on the different systems using adaptive coding and modulation techniques, shows that targets throughputs above 50 Gbps can become a reality for the “Next Generation of Broadband Satellite Systems”, as already mentioned in [1].

REFERENCES